CLAIMS

We claim:

1. A method of forming a ball grid array package, comprising the steps:

providing a semiconductor chip/die;

providing a ball grid substrate; the ball grid substrate having:

a heat spreader with a pattern of slots formed therein; and

a series of balls opposite the heat spreader;

and

affixing the semiconductor chip/die to the ball grid substrate.

2. The method of claim 1, wherein the semiconductor chip/die is a silicon semiconductor chip/die or a germanium semiconductor chip/die.

3. The method of claim 1, wherein the semiconductor chip/die is a silicon semiconductor chip/die.

4. The method of claim 1, wherein the balls are comprised of 63Sn37Pb, 96.5Sn3.5Ag, 5.5Sn3.8Ag0.7Cu or 96.2Sn2.5Ag0.8Cu0.5Sb; and the heat spreader is

comprised of copper, aluminum, chromium plated on copper, chromium plated on aluminum or nickel plated on copper.

5. The method of claim 1, wherein the balls are comprised of 63Sn37Pb or 96.5Sn3.5Ag; and the heat spreader is comprised of nickel plated on copper.

6. The method of claim 1, wherein the balls are comprised of 63Sn37Pb.

7. The method of claim 1, wherein the balls are comprised of 96.5Sn3.5Ag.

8. The method of claim 1, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of from about 2.5 to 3.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

9. The method of claim 1, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of about 2.8; and the heat spreader has a coefficient of thermal expansion of about 17.0.

10. The method of claim 1, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of from about

5.5 to 6.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

11. The method of claim 1, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of about 6.1; and the heat spreader has a coefficient of thermal expansion of about 17.0.

12. The method of claim 1, wherein the slots penetrate the heat spreader from about 25 to 85%.

13. The method of claim 1, wherein the slots penetrate the heat spreader from about 50 to 75%.

14. The method of claim 1, wherein the pattern of slots include rows spaced apart from about 1.0 to 5.0 mm; the slots comprising each row are spaced apart from each other from about 0.5 to 2.5 mm.

15. The method of claim 1, wherein the pattern of slots include rows spaced apart from about 1.5 to 2.5 mm; the slots comprising each row are spaced apart from each other from about 0.7 to 1.5 mm.

16. The method of claim 1, wherein the pattern of slots are arranged in: parallel/perpendicular rows; a circular pattern; a radiating pattern; a rectangular pattern, a square pattern, a concentric circular pattern, a concentric square pattern, or a concentric octagonal pattern.

17. The method of claim 1, wherein the pattern of slots 28 are arranged in parallel/perpendicular rows.

18. The method of claim 1, wherein the ball grid array package is a super ball grid array package, an HSBGA package or an HSFCBGA.

19. The method of claim 1, wherein the ball grid array package is a super ball grid array package.

20. A method of forming a ball grid array package, comprising the steps:

providing a semiconductor chip/die;

providing a ball grid substrate; the ball grid substrate having:

a heat spreader with a pattern of slots formed therein; wherein the slots penetrate the heat spreader from about 25 to 85%; and

a series of balls opposite the heat spreader;

and

affixing the semiconductor chip/die to the ball grid substrate.

21. The method of claim 20, wherein the semiconductor chip/die is a silicon semiconductor chip/die or a germanium semiconductor chip/die.

22. The method of claim 20, wherein the semiconductor chip/die is a silicon semiconductor chip/die.

23. The method of claim 20, wherein the balls are comprised of 63Sn37Pb, 96.5Sn3.5Ag, 5.5Sn3.8Ag0.7Cu or 96.2Sn2.5Ag0.8Cu0.5Sb; and the heat spreader is comprised of copper, aluminum, chromium plated on copper, chromium plated on aluminum or nickel plated on copper.

24. The method of claim 20, wherein the balls are comprised of 63Sn37Pb or 96.5Sn3.5Ag; and the heat spreader is comprised of nickel plated on copper.

25. The method of claim 20, wherein the balls are comprised of 63Sn37Pb.

26. The method of claim 20, wherein the balls are comprised of 96.5Sn3.5Ag.

27. The method of claim 20, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of from about 2.5 to 3.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

28. The method of claim 20, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of about 2.8; and the heat spreader has a coefficient of thermal expansion of about 17.0.

29. The method of claim 20, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of from about 5.5 to 6.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

30. The method of claim 20, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of about 6.1; and the heat spreader has a coefficient of thermal expansion of about 17.0.

31. The method of claim 20, wherein the slots penetrate the heat spreader from about 50 to 75%.

32. The method of claim 20, wherein the pattern of slots include rows spaced apart from about 1.0 to 5.0 mm; the slots comprising each row are spaced apart from each other from about 0.5 to 2.5 mm.

33. The method of claim 20, wherein the pattern of slots include rows spaced apart from about 1.5 to 2.5 mm; the slots comprising each row are spaced apart from each other from about 0.7 to 1.5 mm.

34. The method of claim 20, wherein the pattern of slots are arranged in: perpendicular/perpendicular rows; a circular pattern; a radiating pattern; a rectangular pattern, a square pattern, a concentric circular pattern, a concentric square pattern, or a concentric octagonal pattern.

35. The method of claim 20, wherein the pattern of slots 28 are arranged in parallel/perpendicular rows.

36. The method of claim 20, wherein the ball grid array package is a super ball grid array package, an HSBGA package or an HSFCBGA.

37. The method of claim 20, wherein the ball grid array package is a super ball grid array package.

38. An ball grid array package, comprising:

a semiconductor chip/die affixed to a ball grid substrate; the ball grid substrate having a series of balls; and

a heat spreader mounted to the semiconductor chip/die and the ball grid substrate opposite the series of balls; the heat spreader having a pattern of slots therein.

39. The structure of claim 38, wherein the semiconductor chip is a silicon semiconductor chip or a germanium semiconductor chip.

40. The structure of claim 38, wherein the semiconductor chip is a silicon semiconductor chip.

41. The structure of claim 38, wherein the balls are comprised of 63Sn37Pb, 96.5Sn3.5Ag, 5.5Sn3.8Ag0.7Cu or 96.2Sn2.5Ag0.8Cu0.5Sb; and the heat spreader is comprised of copper, aluminum, chromium plated on copper, chromium plated on aluminum or nickel plated on copper.

42. The structure of claim 38, wherein the balls are comprised of 63Sn37Pb or 96.5Sn3.5Ag; and the heat spreader is comprised of nickel plated on copper.

43. The structure of claim 38, wherein the balls are comprised of 63Sn37Pb.

44. The structure of claim 38, wherein the balls are comprised of 96.5Sn3.5Ag.

45. The structure of claim 38, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of from about 2.5 to 3.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

46. The structure of claim 38, wherein the semiconductor chip/die is a silicon semiconductor chip/die and has a coefficient of thermal expansion of about 2.8; and the heat spreader has a coefficient of thermal expansion of about 17.0.

47. The structure of claim 38, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of from about 5.5 to 6.5; and the heat spreader has a coefficient of thermal expansion of from about 10 to 25.

48. The structure of claim 38, wherein the semiconductor chip/die is a germanium semiconductor chip/die and has a coefficient of thermal expansion of about 6.1; and the heat spreader has a coefficient of thermal expansion of about 17.0.

49. The structure of claim 38, wherein the slots penetrate the heat spreader from about 25 to 85%.

50. The structure of claim 38, wherein the slots penetrate the heat spreader from about 50 to 75%.

51. The structure of claim 38, wherein the pattern of slots include rows spaced apart from about 1.0 to 5.0 mm; the slots 28 comprising each row are spaced apart from each other from about 0.5 to 2.5 mm.

52. The structure of claim 38, wherein the pattern of slots include rows spaced apart from about 1.5 to 2.5 mm; the slots comprising each row are spaced apart from each other from about 0.7 to 1.5 mm.

53. The structure of claim 38, wherein the pattern of slots 28 are arranged in: perpendicular/perpendicular rows; a circular pattern; a radiating pattern; a

rectangular pattern, a square pattern, a concentric circular pattern, a concentric square pattern, or a concentric octagonal pattern.

54. The structure of claim 38, wherein the pattern of slots 28 are arranged in: parallel/perpendicular rows.

55. The structure of claim 38, wherein the ball grid array package is a super ball grid array package, an HSBGA package or an HSFCBGA.

56. The structure of claim 38, wherein the ball grid array package is a super ball grid array package.